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EXAMINER

NGUYEN, CUONG QUANG

ART UNIT

PAPER NUMBER

2811

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/052,266	<b>Applicant(s)</b> IWAMOTO ET AL.	
	<b>Examiner</b> Cuong Q Nguyen	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☐ Responsive to communication(s) filed on \_\_\_\_.

2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_ is/are allowed.

6) ☒ Claim(s) 1-15 is/are rejected.

7) ☐ Claim(s) \_\_\_\_ is/are objected to.

8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All   b) ☐ Some \* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s) ____ 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other:
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## **DETAILED ACTION**

### **Specification**

1. Claim 4-15, objected to because of the following informalities:

A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim 4-15 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim 4-15. See MPEP § 608.01(n). Accordingly, the claim 4-15 not been further treated on the merits.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "electrode layer" in line 5. There is insufficient antecedent basis for this limitation in the claim.

### **Claim Rejections - 35 USC § 102**

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ellul et al. (US 5,394,000).

Regarding claims 1, 2, 3, Ellul et al. discloses a semiconductor device comprising : a planar semiconductor substrate (60) (a semiconductor base body); a substrate buried type capacitor structure with a three-dimensional cavity formed in the planar semiconductor substrate, wherein capacitor structure is formed in a cavity in the substrate in such a manner that an aperture is opened on a surface side of the substrate and that it extends to the middle of the substrate. See Ellul et al.'s Fig.7C.

Regarding claim 4, as shown in Ellul et al.'s Fig.7C, the front surface of substrate and the inner surface of the cavity thereof are constructed by an insulator (62, 78).

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Regarding claims 7, 8, as shown in Ellul et al.'s Fig.7C, the capacitor structure is a laminate structure being formed in the cavity comprising a first electrode layer (82), a dielectric layer (88), and a second electrode layer (90).

Regarding claim 10, Fig.7C does not explicitly shown the capacitor structure connecting to a power source or a ground (GND). It is noted that, in order to make the capacitor operating, a power supply has to connect to the capacitor. So, it is inherent that, the capacitor in Ellul et al. has to connect to a power source or GND.

Claims 1-4, 7-8, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Henkels et al. (US 5,780,335).

Regarding claims 1, 2, 3, Henkels et al. discloses a semiconductor device comprising : a semiconductor base body) having a planar semiconductor substrate (14); a substrate buried type capacitor structure with a three-dimensional cavity formed in the planar semiconductor substrate, wherein capacitor structure is formed in a cavity in the substrate in such a manner that an aperture is opened on a surface side of the substrate and that it extends to the middle of the substrate. See Henkels et al.'s Fig.2C.

Rergarding claim 4, as shown in Henkels et al.'s Fig.2C, the front surface of substrate and the inner surface of the cavity thereof are constructed by an insulator (22).

Regarding claims 7, 8, as shown in Henkels et al.'s Fig.2C, the capacitor structure is a laminate structure being formed in the cavity comprising a first electrode layer (18), a dielectric layer (20), and a second electrode layer (16).

Regarding claim 10, Henkels et al.'s Fig. 2C does not explicitly shown the capacitor structure connecting to a power source or a ground (GND). It is noted that, in order to make the capacitor operating, a power supply has to connect to the capacitor. So, it is inherent that, the capacitor in Ellul et al. has to connect to a power source or GND.

Regarding claim 12, as shown in Henkels et al.'s Fig.2C and Fig.3, a conductive layer (36) is considered as an input/out pad because it provides informations or read informations between the capacitor structure and a transistor in a memory cell. It is noted that the capacitor structure is arranged just under or in the periphery of the input/output pad (36) connected to the substrate.

### **Claim Rejections - 35 USC § 103**

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims are 1-10 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (US 6,184,060) in view of Frankeny et al. (US 5,745,333).

Regarding claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 13, Siniaguine discloses a vertical integrated circuit semiconductor device having a laminate module structure comprising:

a plurality of semiconductor base bodies stacking layers and ball bodies (210) are arranged interposed among the semiconductor base bodies; each of semiconductor having a planar semiconductor substrate (110); a capacitor part formed in the semiconductor substrate (col.2 lines 26-31); a three-dimensional cavity having an approximately truncated-cone shape formed in the semiconductor substrate with its aperture opened on the front surface of the base body and penetrating through the semiconductor substrate to the back side of the base body, wherein the front surface of semiconductor substrate and the inner surface of the cavity thereof are constructed by an insulator (140); an electrode layer (150) formed in the cavity, wherein the back side surface of semiconductor is removed thereby exposing the electrode layer; . See Siniaguine's Fig.7 to Fig.8B and Fig.10.

Siniaguine teaches that the capacitor part formed in the semiconductor substrate. However, Siniaguine does not explicitly teach the capacitor part in each semiconductor body connects to other capacitor part in other semiconductor body in vertical integrated circuit.

Frankeny et al. discloses a vertical integrated circuit comprising: a plurality of base bodies, each of base bodies including a capacitor part, wherein capacitor parts in the base bodies connected to each other in the vertical integrated circuit. See Frankeny et al.'s Fig.22.

It would have been obvious to one of ordinary skill in the art to connect the capacitors in the base bodies to each other as taught by Frankeny et al. into Siniaguine

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because stackable capacitor structure layers in the vertical integrated circuit provide high capacitance, low resistance and low inductance. See Frankeny et al.'s col.5, lines 27-33.

It is noted that, it also would have been obvious to one of ordinary skill in the art, when connect the capacitors to each other in the vertical integrated circuit as suggested by Frankeny et al., would form the capacitor including a first electrode layer, a dielectric layer, and a second electrode layer in the cavity and the first capacitor electrode is exposed the same manner as the electrode (150). One of ordinary skill in the art have been motivated to do so because it is used the same process in Iniaguine's device.

Regarding claim 10, it is inherent that the capacitor has to connected to a power source or GND in order to make the capacitor operate.

Regarding claims 14 and 15, Siniaguine teach that the ball bodies (210) are formed of solder (col.7 lines 51-53) which is inherently has elasticity property.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Dickson (US 4,214,174).

Ellul et al. teaches all the limitations of claim 1 as shown above but does not explicitly show that the capacitor structure is connected to a clock line.

It is conventional and also taught by Dickson (Fig.1 and col.2 lines 49-55) that the capacitor structure is commonly connected to a clock line in order to form a voltage multiplier circuit.



Therefore, it would have been obvious to one of ordinary skill in the art connecting the capacitor structure to a clock line as taught by Dickson in order to form a voltage multiplier circuit.

The expression "formed by etching" in claim 3, "formed by passivation" in claim 4, "by means of a thin film deposition method" in claim 7, "by trimming" in claim 8 are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324,326(CCPA 1974); *In re Marosi et al.*, 218 USPQ 289,292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

### ***Conclusion***

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The

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Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

8. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.



Cuong Nguyen

Primary examiner

7/9/03